REMARKS

Claims 1-12 are pending in the application and are rejected for non-statutory double patenting and in view of prior art.

Rejections for Double Patenting

Claims 1, 3, 5, 7, 10 and 12 are rejected for obviousness-type double patenting over US patent 6,461,882 (referred to as the '882 patent).

The Office Action indicates claim 1 is obvious from claim 1 of the '882 patent.

Applicants respectfully disagree. Claim 1 of the '882 patent claims a method for detecting faults in an integrated circuit (IC) that performs a transition simulation. The transition simulation determines a "train of transition signal values occurring on various signal lines within" the IC. In contrast to this, claim 1 in the present application claims a method that detects faults in an IC by performing logic simulation. The two types of simulation are not the same and are not obvious variants of one another.

A transition simulation must account for the timing of signal transitions so that accurate results can be obtained. This type of simulation requires considerable processing and takes a relatively long time to perform.

A logic simulation does not need to account for the timing of signal transitions. It considers static logic levels rather than signal transitions. It requires less time to perform.

It would not have been obvious from claim 1 of the '882 patent to detect IC faults using logic simulation.

Similar reasons apply to dependent claims 3, 5 and 7.

The Office Action indicates claim 10 is obvious from claim 5 of the '882 patent.

Applicants respectfully disagree for reasons that are analogous to those discussed above for claim 1. It would not have been obvious from claim 5 of the '882 patent to use a logic simulator as recited in claim 10.

Similar reasons apply to dependent claim 12.

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Rejections Under § 103

Claims 1-12 are rejected under 35 USC § 103 as being unpatentable over US patent 5,321,354 (referred to as "Ooshima") in view of US patent 5,425,036 (referred to as "Liu").

With regard to claim 1, the Office Action indicates that Ooshima teaches all limitations of claim 1 except for "performing a logic simulation of the operation of said semiconductor IC"; that Liu teaches both the simulation and emulation of a target system; and that it would have been obvious to modify the teachings in Ooshima by those disclosed in Liu.

Applicants respectfully disagree because there is no obvious motivation to combine teachings from the two references and because, even when combined, not all claim elements are disclosed or suggested.

Ooshima discloses a method for detecting the quality of a semiconductor device by detecting the static current that flows in a power circuit of the device (see col. 2 lns. 63-67).

Liu discloses a method of verifying the functional correctness of a circuit design using emulation by reconfigurable logic devices, e.g., field programmable gate arrays (FPGA). The disclosed method relies on a "read-back" function that captures internal state information from the reconfigurable device (see col. 2 ln. 66 to col. 3 ln. 2).

The method taught in Liu requires internal state information of an emulation device. The method taught in Ooshima uses static current measurements that are taken externally to an actual device. There is no obvious motivation to combine these teachings.

Furthermore, neither reference discloses or suggests generating a list of faults that are detectable by transient power supply current testing. Ooshima expressly teaches away from this feature. Referring to col. 6, Ooshima states the following:

> ... The static current is a current that flows in the power circuit in a state in which the internal elements are stable and fixed to V_{dd} or V_{ss}, so that it is desirable to measure the static current after a certain period of time, a few micro- to milli-seconds for example, passes after the patterns are applied.

Analogous reasons apply to claim 10. Claims 2-9 and 12 depend on claims 1 and 10, and add further limitations thereto. The reasons discussed above for claim 1 also apply to these dependent claims.

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CONCLUSION

Applicants amend the specification and request reconsideration in view of the discussion set forth above.

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Certificate of Transmission

I certify that this Response to Office Action and any following materials are being transmitted by facsimile on February 19, 2004 to the U.S. Patent and Trademark Office at telephone number (703) 872-9306.

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